

FIG. 1

Patented Oct 19, 2005

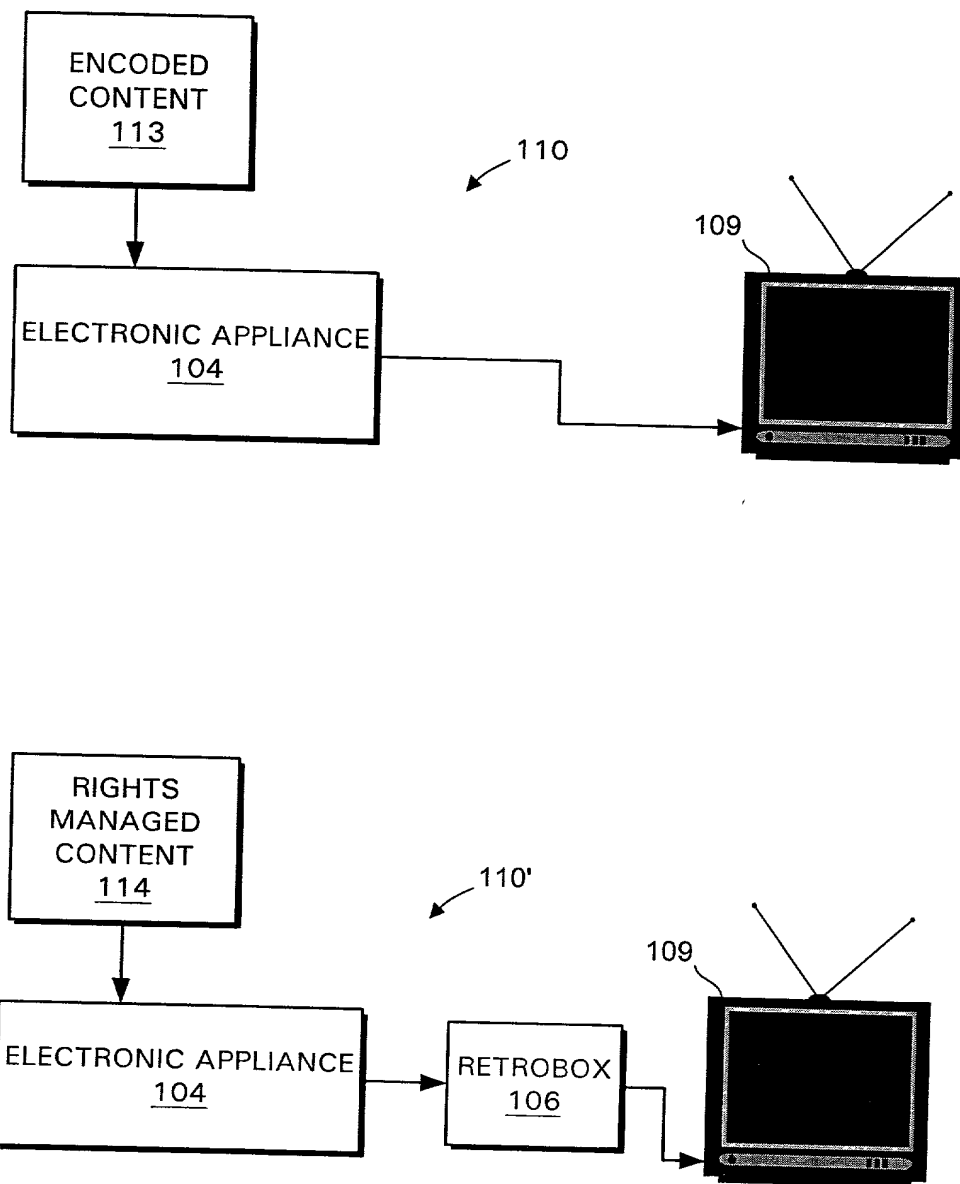


FIG. 1A

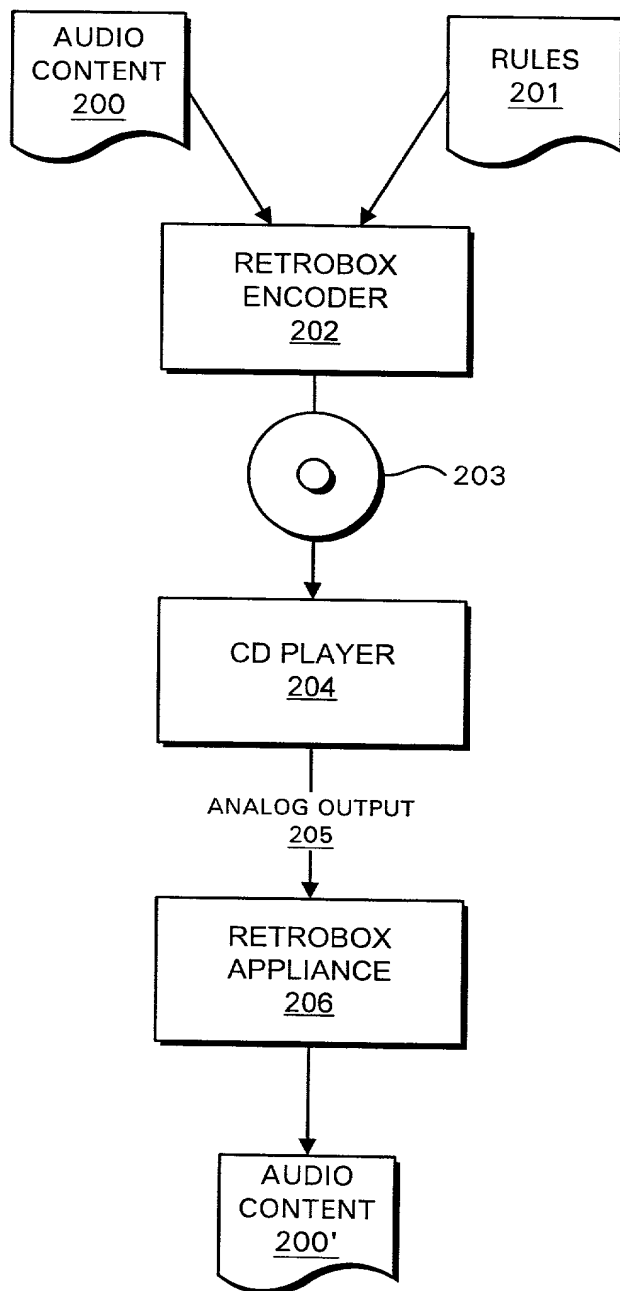


FIG. 2

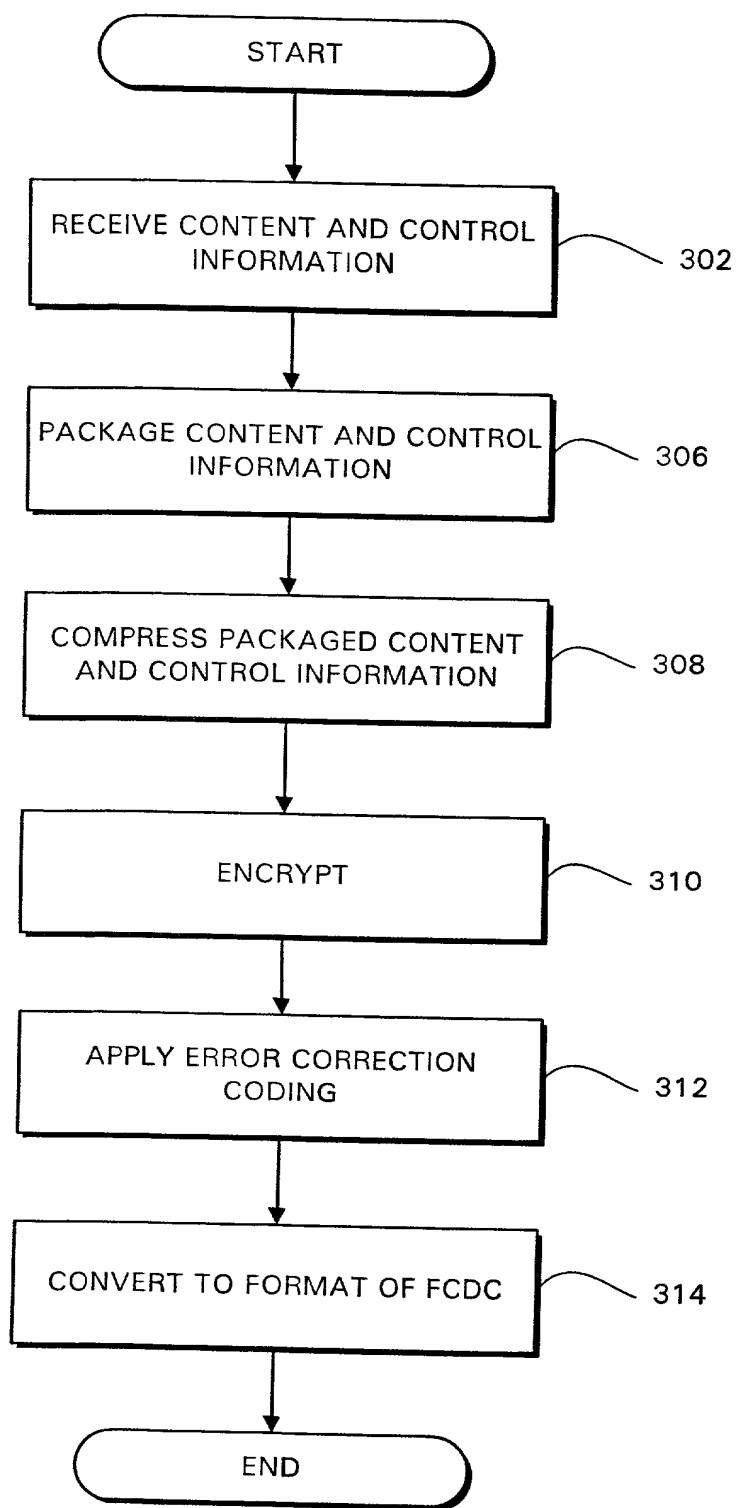


FIG. 3

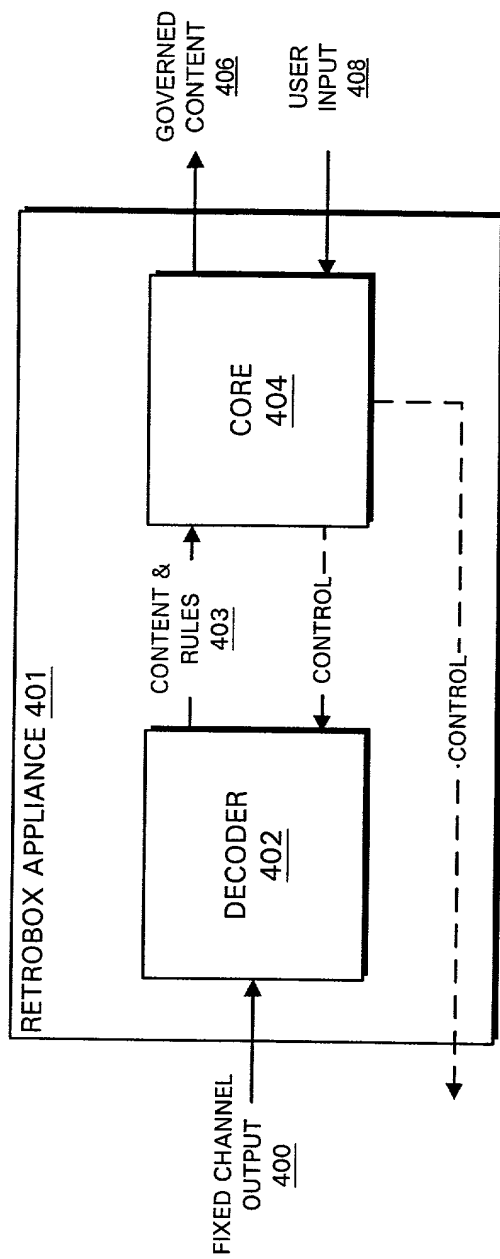


FIG. 4

```
graph TD
    Start([START]) --> Read[Read Input]
    Read --> Sum[Sum = 0]
    Sum --> Loop{ }
    Loop --> Add[Add Input to Sum]
    Add --> Loop
    Loop --> Print[Print Sum]
    Print --> End([END])
```

RECEIVE CODED CONTENT,
CONTROL INFORMATION, AND
NOISE

502

UNFORMAT

504

APPLY ERROR CORRECTION

306

```
graph TD
    A[PLAINTEXT] --> B[ENCRYPT]
    B --> C[ENCRYPTED]
    C --> D[DECRYPT]
    D --> E[PLAINTEXT]
```

508

```

graph TD
    A[ ] --> B[DECOMPRESS]
    B --> C[ ]
    style A fill:none,stroke:none
    style C fill:none,stroke:none

```

510

UNPACK CONTENT AND CONTROL
INFORMATION

512

USE CONTROL INFORMATION TO
GOVERN USE OF CONTENT

514

```

graph TD
    END([END])
  
```

FIG. 5

The diagram illustrates a system 600 with the following components and connections:

- EXTERNAL CONNECTIONS:**
 - NETWORK 620:** A cloud-shaped network connected to the system via a **NETWORK INTERFACE 610**.
 - FROM APPLIANCE LINE OUT - 622:** An input line entering the system from the top right.
 - TO OUTPUT DEVICE:** An output line exiting the system from the bottom.
- INTERNAL COMPONENTS:**
 - SYSTEM MEMORY 604:** A large block containing modules: **RIGHTS MGT -- 629**, **CONTENT RENDERING -- 630**, **DECOMPRESSION -- 634**, and **DECRYPTION -- 632**.
 - CPU 602:** Connected to the SYSTEM MEMORY and the internal bus.
 - SPU 603:** A dashed box representing a Secondary Processor Unit, connected to the internal bus.
 - BUFFER 618:** Connected to the input line and the internal bus.
 - A/D & D/A CONVERSION 619:** Connected to the internal bus and the output line.
- INTERNAL BUS:** A central vertical line (labeled 612) that facilitates data flow between the network interface, buffer, CPU, SPU, and A/D & D/A conversion block.

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